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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,354	03/09/2000	Roy Glenn Musselman		3096

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/522,354	Applicant(s) MUSSELMAN ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10-24-2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-10,13 & 14* is/are rejected.

7)☒ Claim(s) *3, 4, 11, 12, 15 & 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 have been presented for reconsideration in view of Applicant's arguments. Claims 15 and 16 have been presented for Examination.

Drawings

2. The Examiner thanks the Applicant for the submission of the corrected drawings.

Response to Arguments

3. Applicant's arguments filed on 10-24-2003 have been fully considered, the Examiners response is as follows:

3.1 Regarding the 35 U.S.C 103 rejections of Claims 1-14:

Applicants have argued:

> Neither Beausoleil nor DeHon teach or suggest anything remotely similar to "wave logic for producing a plurality of sequential wave signals, each wave signal corresponding to a row of cells and controlling the propagation of logic signals through the cells of the row", which is required by claims 1 and 9.

The Examiner has found applicant's arguments to be persuasive and withdraws the earlier 35 U.S.C. 103(a) rejections of Claims 1-14. An updated search has revealed new art.

Claim Interpretation

4. The claims have been given the broadest interpretation by the examiner. For the purposes of examination the examiner has determined that the term *"wave logic"* refers to a collection of control signals sent to cells in a FPGA that are being used in a processor emulation to enable emulation functionality from the combination of compiled test bench data with actual logic functionality for the purpose of improving the speed of the emulation/simulation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1, 2, 5-10, 13 & 14** are rejected under 35 U. S. C. 103 (a) as being unpatentable over **Beausoleil et al. U.S. Patent 5,551,013** in view of **Sarno et al. U.S. Patent 6,141,636**.

5.1 As regards Independent **Claims 1 and 9** the *Beausoleil et al.* reference discloses; a chip module for an emulation system **(Figures 1-8),** a plurality of logic cells **(Figures 10, 11),** a plurality of input lines **(Figure 7),** a configurable logic function memory element **(Figure 3B),** specifying a logic function of said plurality of input lines **(Figures 1, 2A, 2B, 3A),** that produces an output **(Figures 7 and 10).**

The *Beausoleil et al.* reference does not expressly disclose configurable interconnect logic said configurable interconnection logic routing the output of any cell to an input of any other cell, the plurality of cells arraigned in rows and columns and sequential signals

corresponding to a row of cells and controlling propagation of logic signals through the cells of that row or groups *"wave logic"* signals used to enable emulation resources in the different cells being used for emulation.

The *Beausoleil et al.* reference teaches that software simulation is a slow approach to high-density processor design and therefore there is a need to emulate designs in hardware **(Col. 1 Lines 65-67, Col. 2 Lines 1-3).** An artisan of ordinary skill, would have been motivated to search the emulation art to find a method of improving hardware emulation of high-density processor design. In the same art of processor emulation the *Sarno et al.* reference teaches configurable interconnect logic said configurable interconnection logic routing the output of any cell to an input of any other cell, the plurality of cells arraigned in rows and columns and sequential signals corresponding to a row of cells and controlling propagation of logic signals through the cells of that row **(Figure 1, 2, 14 and 15),** as well as *"wave logic"* signals used to control and reconfigure the emulation resources on an *as needed* basis **(Figure 13, item 102, Figure 16 Items 222 & 220, Figure 18 "EMULATION MEMORY").**

Thus, it would have been obvious, to one of ordinary skill in the art, at the time invention was made, to have combined the processor emulation technologies of the *Beausoleil et al.* reference with the emulation control technologies of the *Sarno et al.* reference because, as electronic circuit designs continue to increase in speed and complexity, it becomes ever more critical to test the developing circuit designs at various stages of development **(Sarbo et al. Col. 1 Lines 42-45).**

5.2 As regards dependent **Claims 2 and 10** the *Beausoleil et al.* reference does not expressly disclose a multiplexer.

The *Sarno et al.* reference discloses a multiplexer **(Figure 3(b) Item 394).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Beausoleil et aL* reference with the *Sarno et al.* reference because *(motivation to combine)* it is desirable to let a user dump desired signals to an external system for analysis and multiplexers allow a user to select which emulation resources they wish to use during a particular emulation test **(*Sarno et al.* Col. 2 Lines 20-23).**

5.3 As regards dependent **Claims 5-8, 13 and 14** the *Beausoleil et al.* reference discloses inputs **(Figure 11)** and outputs **(Figure 10).**

The *Beausoleil et al.* reference does not expressly disclose a strobe (control signal for latching up a signal) or time multiplexing or memory elements feeding into the cell array.

The *Sarno et al.* reference discloses strobe signals and time multiplexing and memory elements feeding into the cell array **(Figures 1, 2 3 Items 354, 350 and 356, memory elements Col. 10 Lines 39-49 and multiplexor Col. 12 Lines 42-51).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Beausoleil et al.* reference with the *Sarno et al.* reference because, the *Sarno et al.* reference provides a method of inserting break points into a hardware emulation **(*Sarno et al Col. 2 Lines 18-22*).**

Allowable Subject Matter

6. **Claims 3, 4, 11, 12, 15 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Claims 1-14 have been presented for reconsideration. Claims 1, 2, 5-10, 13 & 14 have been reconsidered and rejected. Claims 3, 4, 11, 12, 15 & 16 have been objected to.

7.1 This action is **NON-FINAL.**

7.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
January 24, 2004

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100